Elaine Ou

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EDUCATION

Stanford University — Stanford, Calif.
Ph.D. in Electrical Engineering *(GPA: 3.79/4.00)* — *2005 – 2010*
Minor in Management Science and Engineering — *(expected 01/10)*

- National Defense Science and Engineering Graduate Fellow
- Thesis: *Array Architecture for a Nonvolatile 3-Dimensional Cross-point Memory*
- Developed a resistance-change memory architecture from concept to post-fabrication testing

Harvard University — Cambridge, Mass.
M.S. in Computer Science *(GPA: 3.80/4.00)* — *2003 – 2005*

- Teaching Fellow, Lecturer for CS141: Computing Hardware
- Designed and patented a high-speed error-correction circuit implementing asynchronous logic *(US Patent #7546517)*

California Institute of Technology — Pasadena, Calif.
B.S. in Electrical Engineering (with honors) *(GPA: 3.60/4.00)* — *1999 – 2003*

- Doris Perpall Speaking Award for Excellence in Communication (Caltech Undergraduate Research Fellowship)
- Research assistant in Caltech Asynchronous VLSI Group
- Participated in design of asynchronous 80C51 microcontroller
- Developed software tools to automate the optimization of asynchronous memory systems

EXPERIENCE

SanDisk Corporation — Milpitas, Calif.
3D Technology Engineer — *Summer 2008*

- Evaluated prototypes for experimental 3-dimensional memory technology and advised on directions for future implementations

Osha - Liang LLP — Santa Clara, Calif.
Technical Consultant — *2006*

- Provided technical expertise for patent litigation involving Flash memory
- Worked with a team of attorneys to review intellectual property and screen pertinent documents

Intel Corporation — Folsom, Calif.
Flash Products Engineer — *Summer 2004*

- Designed error-correction hardware implementing BCH codes for multilevel Flash memory

Situs Logic — Pasadena, Calif.
Senior Design Engineer — *2003 – 2004*

- Developed CAD tools for asynchronous circuit design and layout
- Designed hardware prototypes to demonstrate asynchronous pulse logic

OTHER

- Fluent in Mandarin
- Strong coding skills in C/C++, Matlab
- Experience with Cadence and Xilinx design tools
- Competitive member of Stanford University Triathlon Team
- Aero Association of Caltech/JPL — Private Pilot; Secretary (2000—2003)
- Captain of the Caltech Flying Team (2001—2003)